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## 教師研究成果資料明細

### SCI、SSCI、A&HCI、EI、TSSCI期刊論文

**1**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2009-01, (已刊登)
Semiconductor Science and Technology 18卷1期:123頁~124頁
A High Performance 80V Smart LDMOS Power Device Based on Thin SOI Technology

**2**.楊紹明(Shao-Ming Yang)、許健(Gene Sheu) ,2009-, (已刊登)
The Ninth International Conference on Electronic Measurement & Instruments
4卷9期:594頁~597頁
Dependence of Breakdown Voltage on Drift Length and Linear Doping Gradients in SOI RESURF LDMOS Devices

**3**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-02, (已刊登)
ECS Transactions 27卷1期:125頁~129頁
Combining 2D and 3D Device Simulations for Optimizing LDMOS Design

**4**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-03, (已刊登)
ECS Transactions 27卷1期:125頁~129頁
Combining 2D and 3D Device Simulations for Optimizing LDMOS Design

**5**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-07, (已刊登)
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An Analytical Model of Surface Electric Field Distributionsin in Ultrahigh-Voltage Metal–Oxide–Semiconductor Devices

**6**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-02, (已刊登)
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Reduction of Kink Effect in SOI LDMOS Structure with Linear Drift Region Thickness

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ECS Transactions 27卷1期:103頁~108頁
Comparison of High Voltage (200-300 Volts) Lateral Power MOSFETs for Power Integrated Circuits

**9**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、陳兆南 ,2010-03, (已刊登)
ECS Transactions 27卷1期:103頁~108頁

Comparison of High Voltage (200-300 Volts) Lateral Power MOSFETs for Power Integrated Circuits

**10**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang)*、張怡楓(Yi-Fong Chang)、曹世昌(Shyh-Chang Tsaur) ,2010-07, (已刊登)
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An Analytical Model of Surface Electric Field Distributions in Ultrahigh-Voltage Buried P-top Lateral Diffused Metal-Oxide-Semiconductor Devices

**11**.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai) ,2010-11, (已刊登)
ICSICT-2006: 2006 8th International Conference on Solid-State and Integrated Circuit Technology, Proceedings 1卷3期:1838頁~1840頁
A 5V/200V SOI Device with a Vertically Linear Graded Drift Region

**12**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、曹世昌(Shyh-Chang Tsaur) ,2009-, ()
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An Analytical Model for Surface Electric Field Distributions in Ultra High Voltage (800V) Buried P-top LDMOS Devices

**13**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang)、曹世昌(Shyh-Chang Tsaur) ,2009-, ()
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**14**.楊紹明(Shao-Ming Yang)、許健(Gene Sheu) ,2009-, ()
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The Reliability of 200V P-channel Silicon-On-Insulator LDMOS on High Side operation

**15**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2009-03, (已刊登)
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A High Performance 80V Smart LDMOS Power Device Based on Thin SOI Technology

**16**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-11, ()
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An 800 Volts High Voltage Interconnection Level Shifter Using Floating Poly Field Plate (FPFP) Method

**17**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-11, (已刊登)
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An 800 Volts High Voltage Interconnection Level Shifter Using Floating Poly Field Plate (FPFP) Method

**18**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-11, ()
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A Novel 800V Multiple RESURF LDMOS Utilizing Linear P-top Rings

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A Novel 800V Multiple RESURF LDMOS Utilizing Linear P-top Rings

**20**.許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2010-10, (已刊登)
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ESD Simulation on GGNMOS for 40V BCD

**21**.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai) ,2011-08, (已刊登)
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Application of Multi-Lateral Double Diffused Field Ring in Ultrahigh-Voltage Device MOS Transistor Design

**22**.蔡宗叡(Jung-Ruey Tsai)、許健(Gene Sheu)、楊紹明(Shao-Ming Yang) ,2011-08, (已刊登)
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Analysis of Si3N4 passivation effect by self-consistent electro-thermal-mechanical simulation in AlGaN/GaN heterostructure HEMTs

**23**.楊紹明(Shao-Ming Yang)、許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai) ,2011-08, (已刊登)
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Effects of SiO2 passivation on AlGaN/GaN HEMT by self-consistent electro-thermal-mechanical simulation

**24**.許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)*、楊紹明(Shao-Ming Yang) ,2011-08, (已刊登)
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Improvement of Electrical Characteristics in LDMOS by the Insertion of PBL and Gate Extended Field Plate Technologies

**25**.許健(Gene Sheu)、蔡宗叡(Jung-Ruey Tsai)*、楊紹明(Shao-Ming Yang) ,2011-08, (已刊登)
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Improvement of Electrical Characteristics in LDMOS by the Insertion of PBL